AMENDMENT TO THE CLAIMS:

1. (Original) A method for manufacturing a thin film transistor, comprising the steps of:

forming a semiconductor film above a substrate;

forming a gate insulating film to cover the semiconductor film;

forming a gate electrode on the gate insulating film;

forming a source region and a drain region in the semiconductor film; and

forming an interlayer insulating film on the gate electrode, wherein

in the formation of the gate electrode, an electrode material layer is layered on the gate insulating film; a mask pattern is formed on the electrode material layer; a first etching process is applied in which the electrode material layer is etched using gas containing fluorine or gas containing a mixture of fluorine and oxygen, and with the mask pattern as a mask to a degree wherein a portion of the electrode material layer remains; and a second etching process is applied in which the electrode material layer is etched using a gas containing a mixture of chlorine and oxygen.

2. (Original) A method for manufacturing a thin film transistor according to Claim 1, wherein

the source region and the drain region are formed by doping impurities into the semiconductor film through the gate insulating film.

3. (Original) A method for manufacturing a thin film transistor according to Claim 1, wherein

the gate insulating film is obtained by layering a SiN film and a SiO_2 film or by forming one of the SiN film and SiO_2 film.

4. (Original) A method for manufacturing a thin film transistor according to Claim 1, wherein

the source region and the drain region are formed by doping impurities into the semiconductor film through the gate insulating film; and

the gate insulating film is obtained by layering a SiN film and a SiO_2 film or by forming one of the SiN film and SiO_2 film.

5. (Original) A method for manufacturing a thin film transistor according to Claim 1, wherein

the gas in the first etching process is produced by mixing fluorine-based gas and oxygen-based gas in an approximately equal volume ratio.

6. (Original) A method for manufacturing a thin film transistor, comprising the steps of:

forming a semiconductor film above a substrate;

forming a gate insulating film to cover the semiconductor film;

forming a gate electrode on the gate insulating film;

forming a source region and a drain region within the semiconductor film; and

forming an interlayer insulating film on the gate electrode, wherein

in the formation of the gate electrode, an electrode material layer is layered on the gate insulating film; a mask pattern is formed on the electrode material layer; and a first etching process and a second etching process are applied to the electrode material layer with the mask pattern made of a resist material as a mask, wherein

in the first etching process, an etching gas having a smaller etching selection ratio between the electrode material layer and the gate insulating film than an etching gas used in the second etching process and having a faster etching rate of the electrode material layer than the etching gas of the second etching process is used, and the electrode material layer is etched to a degree so that a predetermined thickness of the electrode material layer remains in regions not covered by the mask, and

in the second etching process, an etching gas having a larger etching selection ratio between the electrode material layer and the gate insulating film than the etching gas used in the first etching process and having a larger ashing rate of the mask pattern than the etching gas used in the first etching process is used to etch the electrode material layer remaining in the predetermined thickness, so that a gate electrode having a tapered shape wherein the side surface is inclined such that the width becomes narrower toward the upper surface is obtained.

7. (Original) A method for forming a thin film transistor having a semiconductor film and a gate electrode formed above a substrate, the method comprising:

a film forming step for layering an electrode material layer above the substrate;

a first etching step for etching, in a reaction chamber of an inductively coupled plasma

apparatus having an inductively coupled plasma source and a biasing source, at least a portion of the electrode material layer using a mask pattern formed on the electrode material layer as a mask and by activating only the inductively coupled plasma source; and

a second etching step for etching, in a reaction chamber of the inductively coupled plasma apparatus, the electrode material layer which is etched in the first etching step by activating both the inductively coupled plasma source and the biasing source, wherein

a gate electrode having a side surface with a tapered shape is formed.

8. (Original) A method for manufacturing a thin film transistor according to Claim 7, wherein

after a semiconductor film is formed above the substrate, the electrode material layer is formed above the semiconductor film.

9. (Original) A method for manufacturing a thin film transistor according to Claim 8, wherein

after a gate insulating film is formed on the semiconductor film, the electrode material layer is formed on the gate insulating film.

10. (Original) A method for manufacturing a thin film transistor according to Claim 7, wherein

after the side surface of the electrode material layer is formed into a tapered shape through the second etching step, the semiconductor film is formed.

11. (Original) A method for manufacturing a thin film transistor according to Claim 7, wherein

in the first etching step, gas containing fluorine or a gas containing a mixture of fluorine and oxygen is used as the etching gas; and

in the second etching step, a gas containing a mixture of chlorine and oxygen is used as the etching gas.

12. (Original) A method for manufacturing a thin film transistor according to Claim 11, wherein

after a semiconductor film is formed above the substrate, the electrode material layer is formed above the semiconductor film.

13. (Original) A method for manufacturing a thin film transistor according to Claim 11, wherein

after a gate insulating film is formed on the semiconductor film, the electrode material layer is formed on the gate insulating film.

14. (Original) A method for manufacturing a thin film transistor according to Claim 13, wherein

the gate insulating film is obtained by layering a SiN film and a SiO_2 film or by forming one of the SiN film and the SiO_2 film.

15. (Original) A method for manufacturing a thin film transistor according to Claim 11, wherein

after the side surface of the electrode material layer is formed into a tapered shape through the second etching step, the semiconductor film is formed.

16-20. (Canceled)

21. (New) A method for manufacturing a thin film transistor according to Claim 1, wherein the gate electrode has a single-layer structure.

22. (New) A method for manufacturing a thin film transistor according to Claim 6, wherein the gate electrode has a single-layer structure.

23. (New) A method for manufacturing a thin film transistor according to Claim 7, wherein the gate electrode has a single-layer structure.